A High Speed Low Voltage 45nm CMOS Balanced OTA based on Flipped Voltage Follower Current Mirror

Vidhata Poddar[1] and Zoonubiya Ali[2]

[1,2]Disha Institute of management and technology, Raipur (C.G)
E-mail: [1]vidhata.ankur15@gmail.com, [2]zoonubiya.ali@dishamail.com

Abstract—*In this paper a low voltage OTA based on class-AB FVFCM (Flipped voltage Follower current mirror) and a differential pair comprises of both nMOS and pMOS device to achieve high gm/Id ratio and low power operation with sufficient linearity is presented. Flipped voltage follower based current mirror has been widely used for low voltage circuits. Recent design work on OTA low voltage operation suggests that the device size and voltage downscaling can be done, but this reduces the voltage swing. The design, simulation and performance of OTA have carried out under 45nm CMOS technology with a ±0.7V power supply. The tuning of transconductance can be done by varying the supply voltage. Under ±0.7 V supply the transconductor achieves a -3dB frequency of 1.3 GHz and cut-off frequency of above 10 GHz. The linear range is 300mV$_{p-p}$ with transconductance of 12uS to 166µS these properties makes OTA suitable for low power and high speed applications.*

Keywords*: OTA, FVF, pseudo-differential, low-voltage, low-power, input linear range.*

1. INTRODUCTION

CMOS transconductor is an essential part of the high speed and low power sub-systems like ADC, filters, oscillators, VGAs etc, Recent year works[1-4] focus on reducing the supply voltage and power consumed by the OTA so that overall power dissipation of the system of can be effectively reduced.

The transconductor presented in [1] presents a differential CMOS transconductor based on FVF. Linearity of the transconductor is improved by mobility reduction compensation technique and achieves a 0.4V$_{p-p}$ input range. OTA comprised of FVF and source degeneration technique is presented in [2], OTA in [2] achieves 1.1mS of transconductance with 11.8 mW power dissipation. The OTA reported in [3] uses bias offset technique to reduce the power consumption also it employs FVS (Flipped Voltage Sources) as tail current source in source coupled differential pair. The telescopic OTA reported in [4] is designed using 50nm BSIM4v4 with supply voltage of 1V to achieve a UGB of 637 MHz while dissipating 540µW of power but the input range of this OTA is very less.

This work presents a new low voltage low power pseudo differential transconductor. It employs both nMOS and a pMOS in the differential pair. In order to achieve low voltage and low power operation balanced and symmetric pseudo-differential structure with FVFCM (flipped voltage follower) based current mirror is used which uses a biasing voltage of 0.1V.

Section II shows the low voltage FVF based current mirror, and based on this current mirror in low voltage OTA DC simulations are discussed. In section III all the simulations are discussed. Sections IV include the conclusion for the OTA. All the spice simulations are carried out using 45nm CMOS technology PTM model files [6] of BSIM 4v4 parameters in LTspice-IV spice simulator.

2. CURRENT MIRROR AND OTA DC ANALYSIS AND SIMULATION

2.1 FVF (Flipped voltage follower) based current mirror

In Fig 1 Flipped voltage follower is shown it is just a cascode amplifier. It is a negative feedback circuit with series shunt topology [7]. Due to shunt configuration output impedance of FVF is low

$$\text{Zout} = \frac{1}{gm1.gm2\,ro}.$$

Due to low output impedance this circuit is able to sink a large current from the load but is limited to I_B. It requires a low voltage supply ($V_{DDmin}=V_{GS2}+V_{DSsat}$) and provides low static power dissipation [8].

Now in flipped voltage current sensor (FVFCS) in Fig 2 shunt feedback provided by transistor M2 the input impedance at node Vx is very low and in this way the amount of current flows through this node does not modify value of its voltage. FVF translates large current variations at node Vx into

compressed voltage variations at output node Vy, which is nearly constant and can be used to generate replicas of input current.

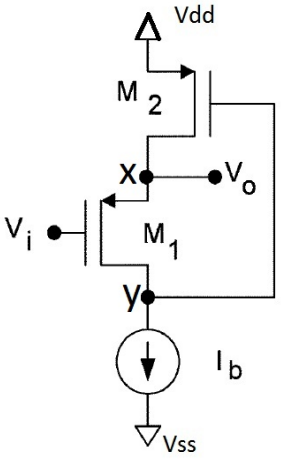

Fig. 1: Flipped voltage follower

Fig. 4 shows the DC simulation result of the flipped voltage follower current sensor (FVFCS), the circuit is simulated for supply voltage of ±0.7 V with basing voltage V_b=0.1 V and for this the input current is varied from -20µA to +20µA.Transistor sizes for M1, M2 and M3 are equal i.e. (2.5µm/50nm). The circuit performs the same operation as discussed above. The voltage at node Vx follows the voltage at node Vy and the output current I_{D3} follows the input current after approaching the biasing current I_B. For the low voltage OTA with very low biasing voltage are needed for low power system. Considering all requirement OTA a current mirror is used in the OTA to route the signal current from input to output. Thus, a low voltage current mirror based on FVF is shown in fig 3.

The biasing voltage required for such current mirror is of the order of V_{DSsat} which can be as small as 0.1V which is much smaller than V_{GS} drop required for conventional low voltage current mirror. The input impedance of the current mirror is low and it is of the order of 20-100Ω.

The minimum supply requirement of such current is of the order of

$$V^{DD}_{min} = |V_{TP}| + 2.V_{DSsat.}$$

When the current transfer ratio form input to output is unity, the circuit in fig 3 operates as current mirror. From the simulation result in fig 5 for FVF based current mirror that this current mirror has the capability of working with low supply voltage and dissipates very less power.

The current mirror in fig 3 uses supply voltage of ±0.7 V with transistor sizes M1 M2 M3 and M4 equal to 2.5µm/50nm and biasing voltage of 0.25V. The input current swept from -150µA to 150µA, the output current vary from -150µA to 150µA, this ensures the circuit to function as a current mirror.

In this current mirror cascoding of M4 is done with M1 to reduce the power dissipation, but still we get some mismatch due to process and second order effects because we are using a channel length of 50nm.

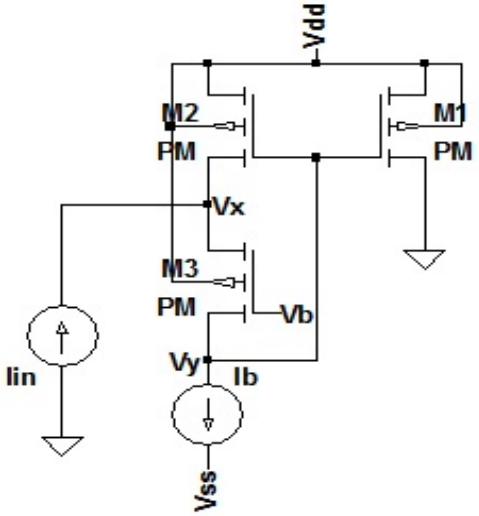

Fig. 2: Flipped voltage current sensor.

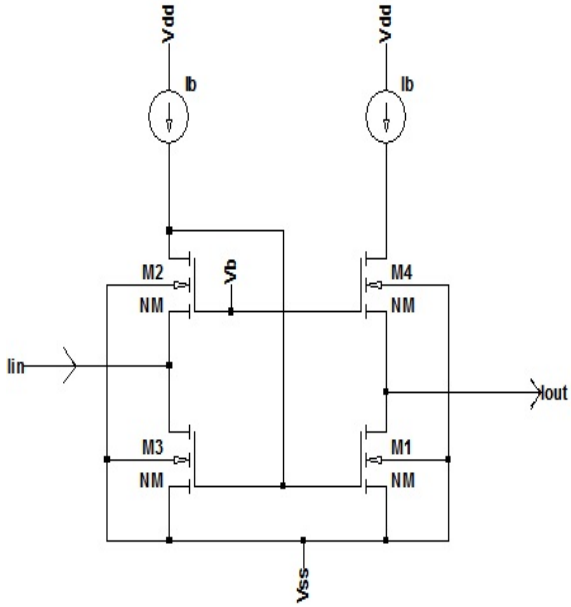

Fig. 3: FVF based current mirror

Based on the FVF current follower current mirror an OTA is presented which works with very low supply voltage. The transconductor is highly linear since it uses class-AB linearization technique also the V_{DSsat} for input transistor is provided by node V_{xp1} and V_{xp1} for both the nMOS and pMOS device. The biasing voltage V_{BN} and V_{BP} required for the operation for current mirror is 0.1V. The biasing current for the current mirror cell is 10 µA for both pMOS and nMOS current mirrors.

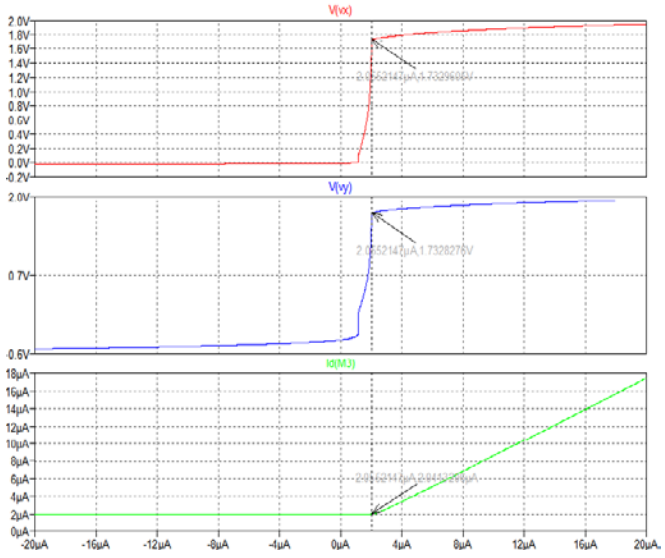

Fig. 1: Simulation result for FVF current sensor

2.2. Overall circuit of OTA

The transconductor makes use of both nMOS and pMOS device in two separate differential pair to form a balanced and symmetric differential transconductor. Due to this the input common mode range increases, thus a particular important feature when low voltage supply is used. When input common mode range is close to positive power supply M2 will turn off and current will flow from M1 and when input common mode range is close to negative power supply M1 turn off and current will flow from M2. The same process will happen in the other half of the circuit but, here the case just opposite since the input terminals are inverted for the nMOS and pMOS device i.e. for M3 and M4. Thus, I_{OUT+} changes in direction opposite to the direction of current I_{OUT-} and the total output current is given by

$$I_{OUT} = I_{O+} - I_{O-}$$

And the input differential voltage is given by

$$V_{id} = V_{in+} - V_{in-}$$

In the transconductor there is pair of two nMOS and two pMOS current mirror the sizes of pMOS devices are equal and nMOS devices are also equal except for the input device since it achieves the overall transconductance. The circuit is capable of operating in high frequency range, since there are less internal nodes in the circuit [11]. All the transistors are biased in saturation region for circuit.

The transconductor cell comprises of symmetric pair of pseudo-differential pair employing both nMOS and pMOS device. The half circuit of overall transconductance cell is shown in fig 6. The source terminal of the transistor nMOS M1 and pMOS M2 are connected to the output nodes Vxn and Vxp FVF current mirror cells. Both the current and voltage of these two cells are mirrored to the output stage. The output current of these cells are I_n and I_p. Thus the output current of these cells are given by

$$Io_+ = Io_- = (gm15 Vyn1 \frac{gm20}{1+gm20}) - (gm11 Vyp1 \frac{gm17}{1+gm17})$$

$$Vyp1 = \sqrt{\frac{2.Id1}{\mu n\ Cox\ (\frac{W}{L})1}} + |Vtp| - Vin-$$

$$Vyn1 = \sqrt{\frac{2.Id1}{\mu n\ Cox\ (\frac{W}{L})2}} + Vtn - Vin+$$

The channel length of the entire nMOS and pMOS devices are chosen to be 50nm, this makes the overall system affected by velocity saturation and channel length modulation. This can produce a high mismatch between calculated and simulated results. Thus, after including the effects of channel length modulation and mobility degradation [9] the drain current equation can be given by

$$I_D = \frac{1}{2} \mu_n C_{ox} (W/L) (V_{eff})^2 (1/(1+(\Theta (V_{eff})^2)^m)^{1/m} (1+\lambda (V_{DS} - V_{eff}))$$

Where, $V_{eff} = V_{GS} - V_{th}$ and Θ is mobility degradation parameter.

Fig 7 shows the overall transconductance made of two equal and symmetrical half circuits. The current of the nMOS current mirrors are cross coupled to minimize the current and voltage offset of the circuit. The advantage of using differential pair in low voltage application is that it avoids the voltage drop across tail current. The transconductor is symmetrical about YY' line as shown in fig 7.

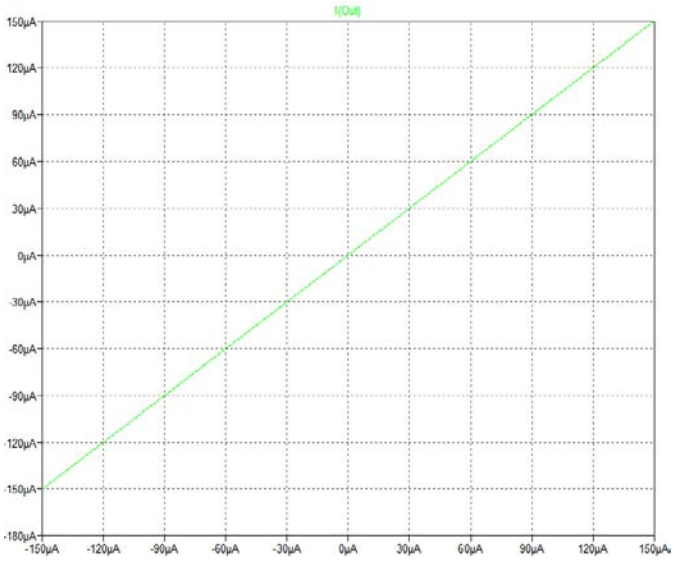

Fig. 2: Simulation result FVF based current mirror

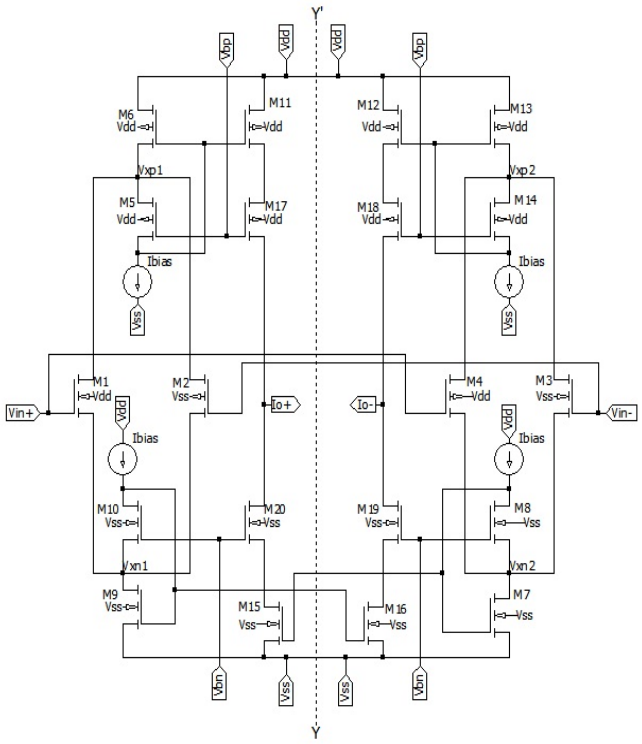

Fig. 3: OTA circuit

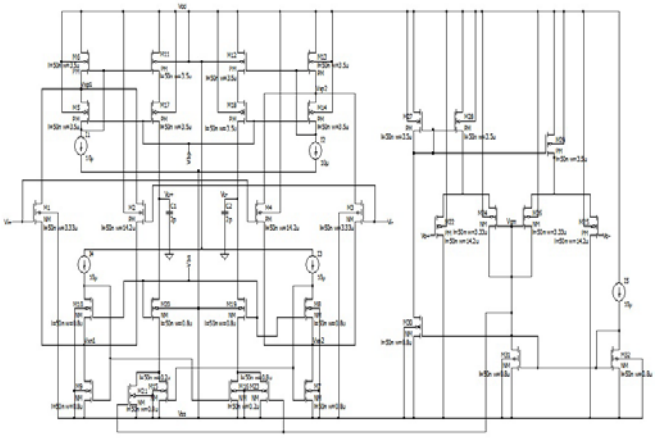

Fig. 4: Overall OTA with output common mode control circuit

3. SIMULATION RESULTS

The pMOS and nMOS FVF current mirror maintains a constant gate source voltage across input differential pairs (M1, M2, M3, and M4) and low impedances at node V_{xni} and V_{xpi}. Where *i* denote differential pair number, in this circuit for left half of differential pair *i*=1 and for the right half *i*=2. When $V_{id}=V_{i+}-V_{i-}$, varies from V_{SS} to V_{DD} the voltages at V_{xni} and V_{xpi} maintains positive and negative voltage separated by the difference of value of nMOS and pMOS threshold voltage level. For $V_{DD}=-V_{SS}$ = 0.7 V and varying the input differential voltage from V_{DD} to V_{SS} the voltages at V_{xp1} changes in opposite direction of V_{xp2}, similarly V_{xn1} changes in opposite direction of V_{xn2} i.e. when xp1 node voltage is pulled up the node voltage of xp1 is pulled down as shown in fig 8.(a & b), the same

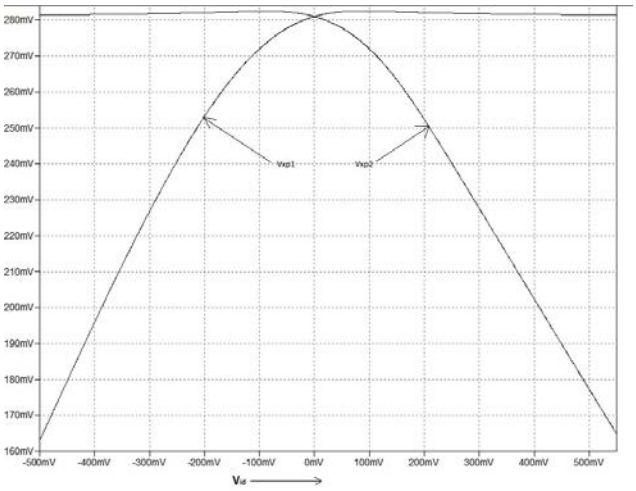

Fig. 8(a): Variation of voltages at xp1 and xp2 w.r.t. Vid.

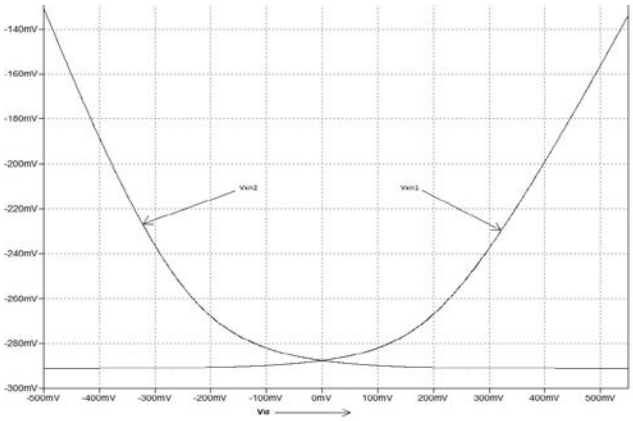

Fig. 8(b): Variation of voltages at xn1 and xn2 w.r.t. Vid.

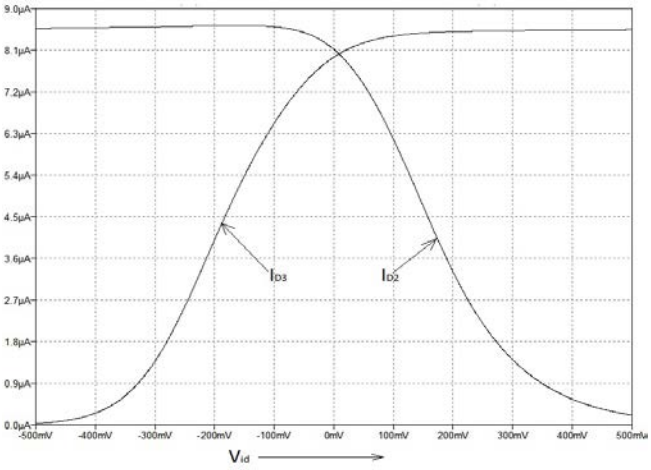

Fig. 8(c): Variation of drain currents of M2 and M3 w.r.t. Vid.

at node xn1 and xn2, this makes the drain current of left input differential pair nMOS to rise in positive direction while the pMOS transistor in right input differential pair to rise in negative direction until the devices get out of saturation. The output current I_{out+} and I_{out-} also changes in opposite direction due the differential action as shown in fig 8. (c & d). The individual and total output current change on variation of Vid can be shown as fig 9. This current variation can be varied in accordance with supply voltage V_{DD} this also varies the transconductance of the circuit as shown in fig 10 (a & b).

When Vid=0, $I_{D17} = I_{D20} = K_P\ [2(V_{cm})^2 - V_{thn}\ (2\text{-}V_{thn})\text{-}V_{thp}\ (2\text{-}V_{thp})]$ and $I_{out+} = I_{out-} = 0$.

But when V_{id} varies $I_{out-} = -I_{out+} = 2\ (I_{D17} - I_{D20})$. This analysis is for left half circuit same will be applied to right half circuit.

Gm = [Iout/Vid] and $I_{OUT} = (I_{OUT+}.I_{OUT-}) = 2I_{out+}$

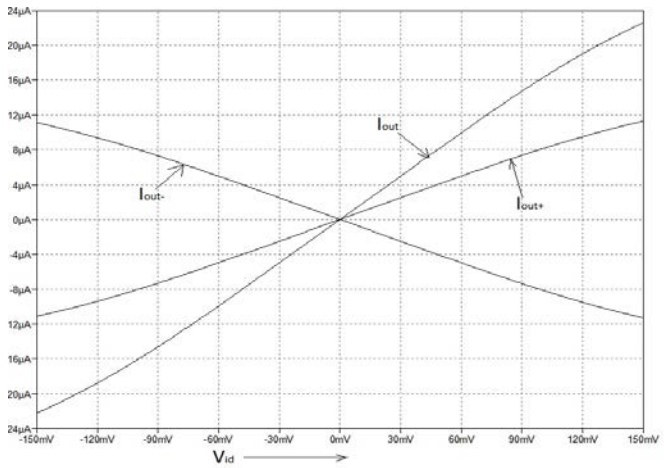

Fig. 9: Variation of output currents Iout+ and Iout- and total output current (Iout+ - Iout-) w.r.t. Vid

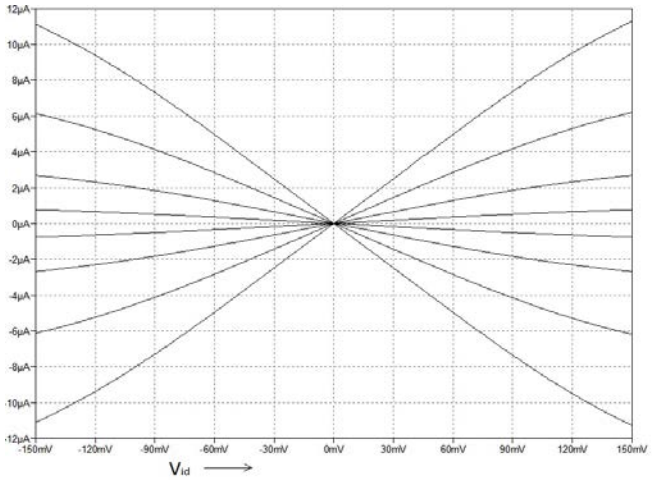

Fig. 10(a): Variation of output currents Iout+ and Iout- w.r.t. Vid and V_{DD}

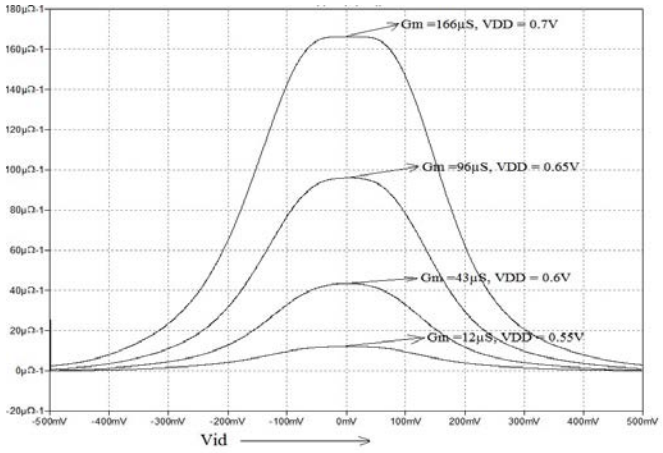

Fig. 10(b): Variation of transconductance w.r.t. Vid and VDD

The frequency response of the OTA is shown in fig 11. The output differential voltage for the circuit is simulated for 0.2pF load capacitor, fig 11 shows that the differential output of the OTA achieves a transition frequency of 104MHz and a phase margin of 60˚ at the same time its cutoff frequency reaches more than 5GHz. At a frequency of 1GHz the of the OTA reaches -18dB with the phase of 118˚.

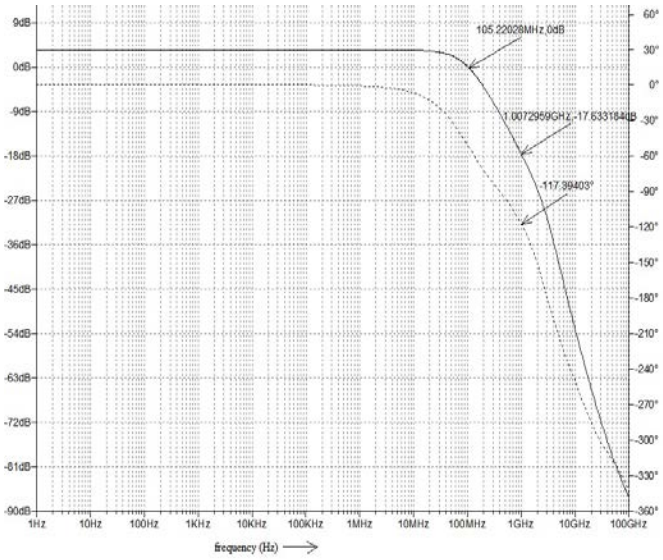

Fig. 51: Frequency response of the transconductor.

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4. SECOND AND FOLLOWING PAGES

The input referred noise voltage for the OTA for 2pF load is simulated from the simulation results it is clear that due to common mode circuit noise performance of the OTA is excellent, and at 100MHz is found to be 47nV/$\sqrt{Hz}$ and the output noise is extremely low, it is 2nV/$\sqrt{Hz}$.Now, for the an input of 100mV$_{p-p}$ the output current is 10µA$_{p-p}$ as shown in fig 12. Fig 13 shows the transient behavior of the OTA for an input step of 200mV$_{p-p}$ the output differential voltage across 2pF capacitor load is obtained to be 600mV. Table 1 shows the total harmonic distortion of the OTA for input differential voltages of 100mVp-p at 1MHz for 2pF capacitor load the, first 9 harmonics is only 1.5%. In all the cases for simulation the supply voltage is kept at ±0.7V. The static power dissipation of overall circuit is only 90µW.

Table 1: THD results for the OTA

Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component	Phase [degree]	Normalized Phase [deg]
1	1.000e+06	1.885e-01	1.000e+00	-19.06°	0.00°
2	2.000e+06	5.770e-04	3.061e-03	-96.56°	-77.51°
3	3.000e+06	2.771e-03	1.470e-02	-49.11°	-30.05°
4	4.000e+06	3.132e-05	1.661e-04	-171.50°	-152.45°
5	5.000e+06	8.677e-05	4.602e-04	5.37°	24.43°
6	6.000e+06	8.316e-06	4.411e-05	-93.07°	-74.01°
7	7.000e+06	3.607e-05	1.913e-04	-121.37°	-102.31°
8	8.000e+06	3.442e-06	1.826e-05	-58.31°	-39.26°
9	9.000e+06	4.602e-06	2.441e-05	-63.91°	-44.86°

Total Harmonic Distortion: 1.502344 %(1.503060%)

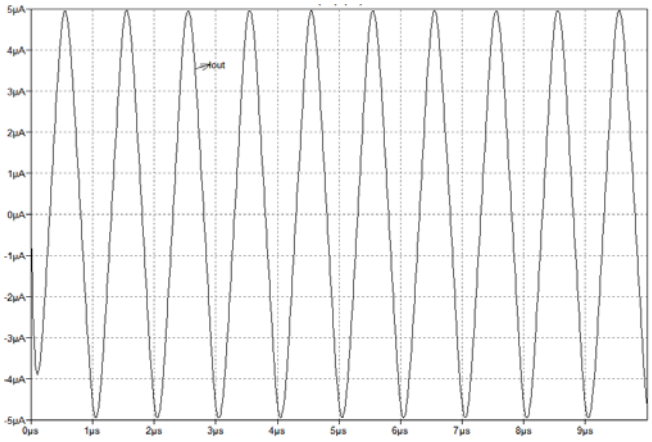

Fig. 62: Output differential current.

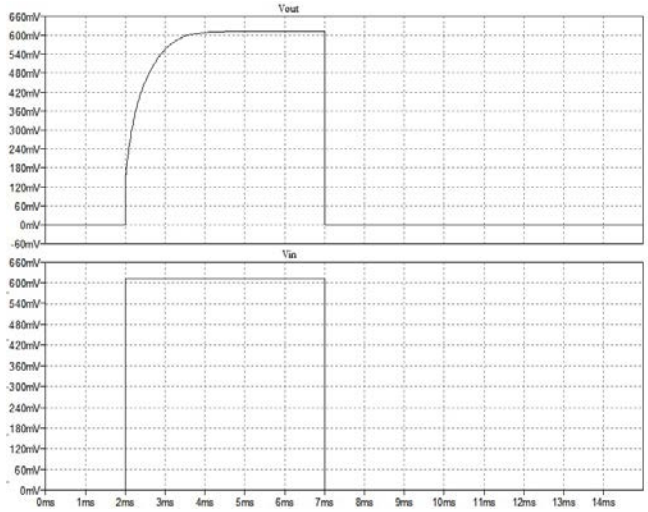

Fig. 73: Transient response of OTA for step input

Table 2 shows the performance comparison results w.r.t to the previous work in order to have a clear outcome of the results. The W/L ratio of the nMOS and pMOS device used in this OTA is summarized in terms of their respective application and type in Table 3.

Table 2: Comparison with previous work

PARAMETER	Ref.[1]	Ref.[2]	Ref.[3]	Ref.[4]	This Work
Supply	1V	1.8V	±0.9V	1V	±0.7V
Technology	130nm	180nm	180nm	50nm	45nm
Power Dissipation	345µW	11.8µW	57µW	560µW	90 µW
Transconductance	88µS	1.1mS	25µS	-	12µS-166 µS

Tuning Capability	Yes	Yes	Yes	No	Yes
Input referred noise	30nnV/$\sqrt{Hz}$	1.3μ/$\sqrt{Hz}$	-	-	47nV/$\sqrt{Hz}$
Input swing range	400mV_{p-p}	0.85V_{p-p}	0.8 V_{p-p}	350 mV_{p-p}	200mV_{p-p}
Transconductance Tuning Method	Voltage Tuning circuit	Biasing current	Biasing current	-	By varying supply

Table 3: Transistor sizing for the OTA

Transistor type	Transistor number	W/L ratio
nMOS OTA	NM(7,8,9,10, 15,16,19,20)	0.8μm/50nm
pMOS OTA	PM(5,6,11,12,13,14,17,18)	3.5μm/50nm
nMOS OTA	NM(1,3)	3.33μm/50nm
pMOS OTA	PM(2,4)	14.2μm/50nm
nMOS CMFB	NM(24,26)	3.33μm/50nm
pMOS CMFB	PM(22,25)	14.2μm/50nm
nMOS CMFB	NM(30,31,32)	0.8μm/50nm
pMOS CMFB	PM(27,28,29)	3.5μm/50nm
nMOS CMFB	NM(21,23)	0.2μm/50nm

The entire transistor sizing used and the simulation results are done on the basis of the fact that mobility of electron and hole ratio μ_n/μ_p=3(approx.), but by including the second order effect has forced us to for further some optimizations.

Comparison results show that the scaling the device size and the operating voltage with the use of Flipped voltage follower current mirror obtain overall better results from the previous results. The disadvantage here is that this circuit lacks with sufficient input voltage swing, but the other parameters are still in good compromise.

5. CONCLUSION

In this paper an OTA with optimized results is presented, this OTA has a better performance in terms of power consumption and supply voltage which was the important factor while designing the OTA. FVF Current mirror used in this OTA with simply cascoding the output stage of the OTA results low power. The whole circuit is designed under ±0.7V 45nm technology which also results in better area efficiency for its implementation. There are some tradeoffs between in terms of linearity, power dissipation and area which are unavoidable after some limit and will result design changes.

REFERENCE

[1] Tamer farouk, Ahmed Nader mohieldin, Ahmed hussain khalil "A low voltage low power CMOS fully differential linear transconductor with mobility reduction compensation" microelectronics journal 43(2012) pg no. 69-76.

[2] X. Zhu and Y.Son "low distortion low voltage operational transconductance amplifier" IEEE Electronics Letters (Volume: 44, Issue: 25), Dec. 2008.

[3] Fujihiko matsumoto, Toshio Miyazawa, Shintaro nakamura yashuaki naguchi "Techniques for low voltage low power linear MOS transconductor" IEEE IPSACS 2008.

[4] Hoang Trang, Pham Xuan Hoang ,Trang Hoang quan, "A Novel design of low power, high speed OTA in 50nm- CMOS technology" IEEE ISSPIT 2012.

[5] Ramon Gonzales Carvajal, Jamie Ramirez angulo, Antonio J. Lopez martin, Antonio Torralba, Juan Antonio Gomez galan, Alfonzo Carlosena, Fernanado Munoz Chavero, "The flipped voltage follower: A useful cell for low voltage low power circuit design" IEEE trans. On circuit and system-I regular papers, Vol.2, No.57, 2005.

[6] www.ptm.asu.edu

[7] Maneesha gupta, urvashi singh "A new flipped voltage follower with enhanced bandwidth and low output impedance" Analog Integr Circ Sig Process (2012) 72:279–288.

[8] Ali assi and Mohamad sawan "High performance CMOS transconductor for Mixed signal analog-digital application" Analog Integrated Circuits and Signal Processing, Vol. 19, 303-317 (1999).

[9] D.A Jones and K.W. Martin "Analog integrated circuit design" John Wiley and sons, 2012, 2nd ed.

[10] R. J. Baker, "CMOS circuit design, layout and simulation" 3rd ed. IEEE press john wiley and sons.

[11] Bram Nauta, "Analog Cmos Filters for very high frequency" Kluwer academic publisher, 1993.